

10 →

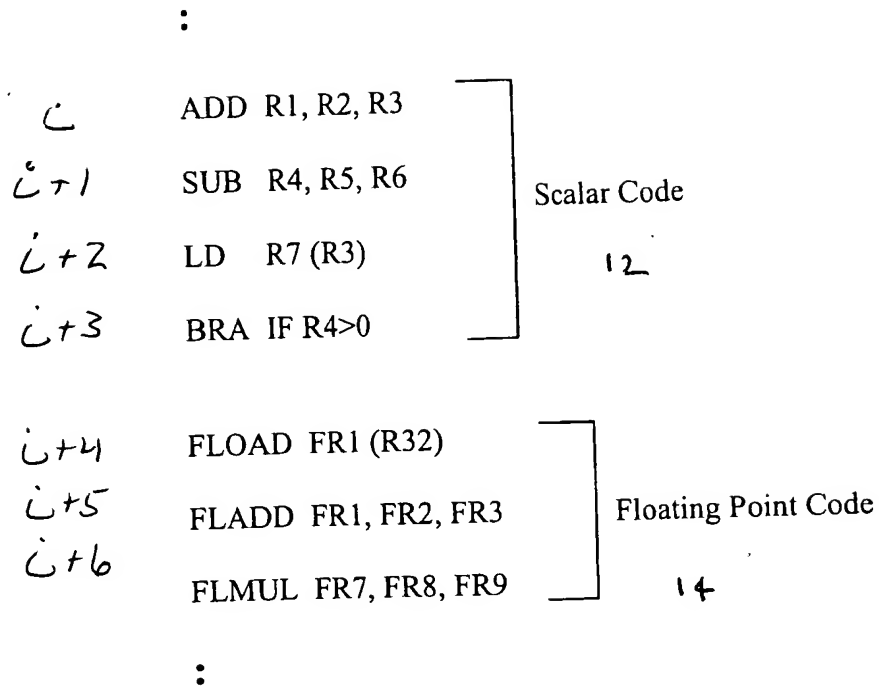


FIG. 1

20 →

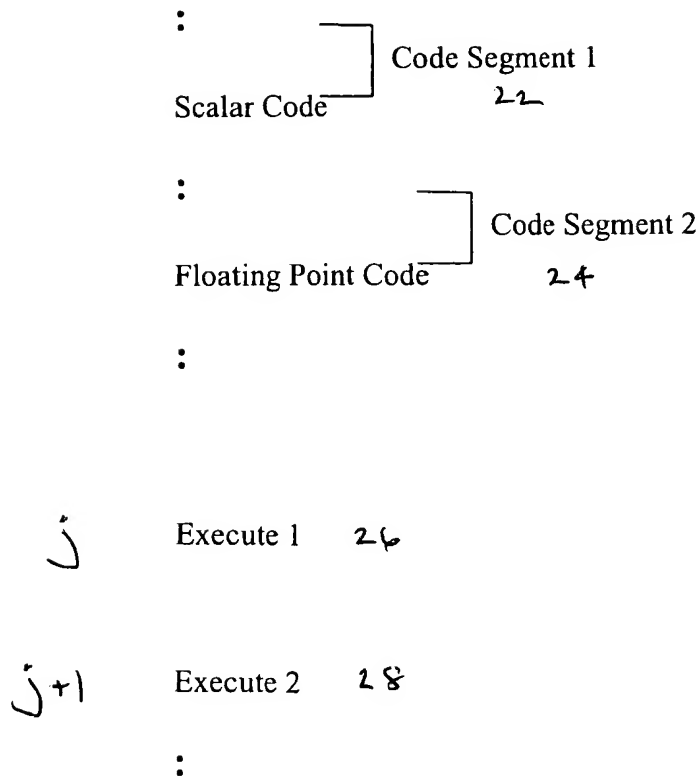


FIG. 2

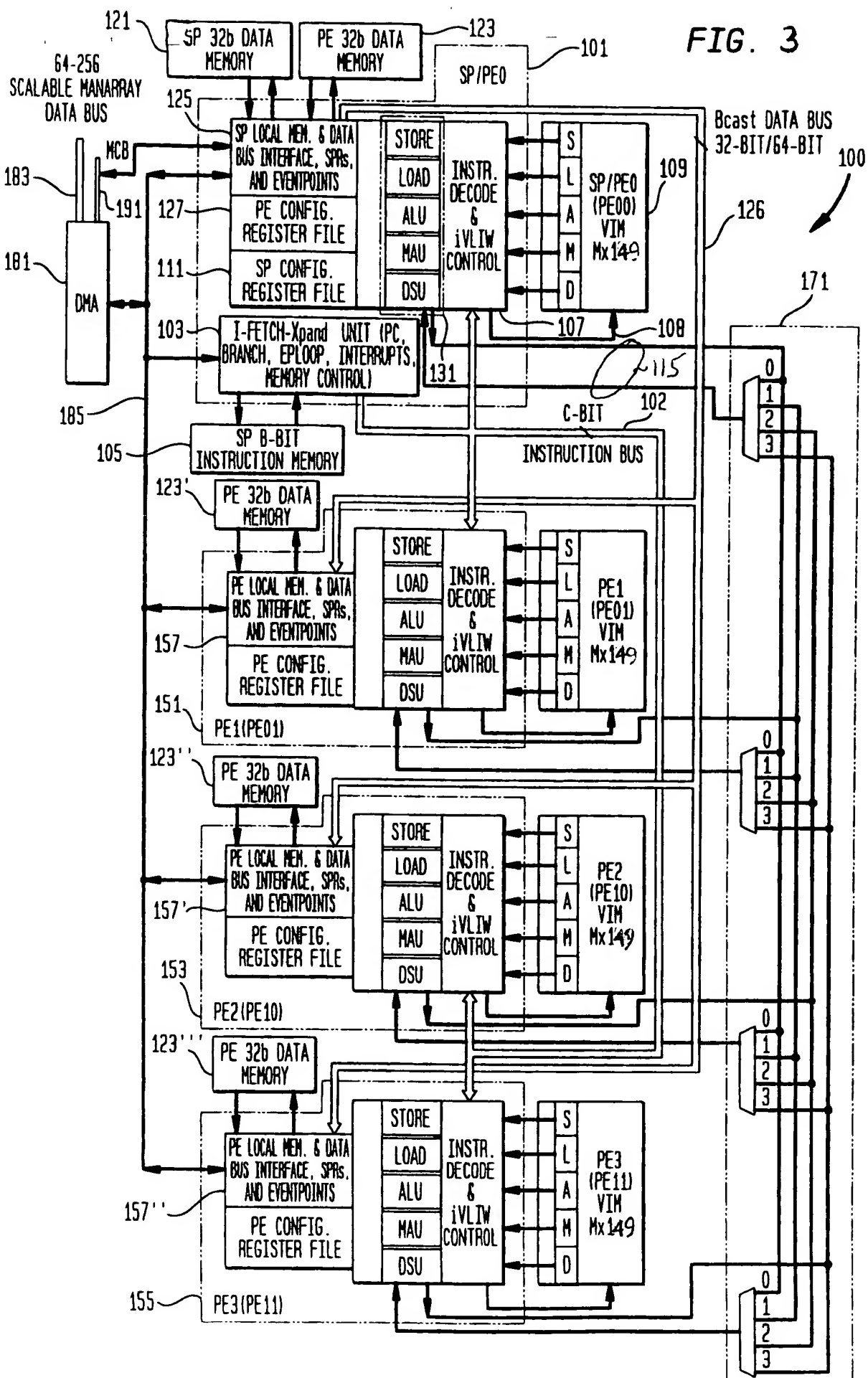
FIG. 3 is a block diagram of a Scalable Manarray architecture. The system consists of four parallel processing elements (PE0, PE1, PE2, PE3) connected to a common data bus (126) and a DMA unit (181).

Common Components:

- 64-256 SCALABLE MANARRAY DATA BUS (121):** Connects to the DMA unit (181) and the SP/PE0 (101) block.
- DMA (181):** Data Movement Accelerator, connected to the data bus (121) and the MCB (191).
- MCB (191):** Memory Control Block, connected to the data bus (121) and the SP/PE0 (101) block.
- SP/PE0 (101):** Shared Processing Element/Processing Element 0, containing:
 - SP 32b DATA MEMORY (121):** Shared Processing Element 32-bit Data Memory.
 - PE 32b DATA MEMORY (123):** Processing Element 32-bit Data Memory.
 - SP LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS (125):** Shared Processing Element Local Memory & Data Bus Interface, Shared Processing Element Registers, and Event Points.
 - PE CONFIG. REGISTER FILE (127):** Processing Element Configuration Register File.
 - SP CONFIG. REGISTER FILE (111):** Shared Processing Element Configuration Register File.
 - STORE, LOAD, ALU, MAU, DSU:** Store, Load, Arithmetic Logic Unit, Memory Access Unit, and Data Stream Unit.
 - INSTR. DECODE & iVLW CONTROL (107):** Instruction Decode & Instruction Value Logic Word Control.
 - SP/PE0 (PE00) VIM Mx149 (109):** Shared Processing Element/Processing Element 0 Vector Instruction Memory Mx149.
- I-FETCH-Xpand UNIT (103):** Instruction Fetch-Expand Unit (PC, BRANCH, EPLOOP, INTERRUPTS, MEMORY CONTROL).
- SP B-BIT INSTRUCTION MEMORY (105):** Shared Processing Element B-Bit Instruction Memory.
- PE 32b DATA MEMORY (123'): (PE1, PE2, PE3):** Processing Element 32-bit Data Memory for each PE.
- PE LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS (157): (PE1, PE2, PE3):** Processing Element Local Memory & Data Bus Interface, Processing Element Registers, and Event Points for each PE.
- PE CONFIG. REGISTER FILE (151): (PE1, PE2, PE3):** Processing Element Configuration Register File for each PE.
- STORE, LOAD, ALU, MAU, DSU:** Store, Load, Arithmetic Logic Unit, Memory Access Unit, and Data Stream Unit for each PE.
- INSTR. DECODE & iVLW CONTROL (107):** Instruction Decode & Instruction Value Logic Word Control for each PE.
- PE1 (PE01) VIM Mx149 (108):** Processing Element 1 (PE01) Vector Instruction Memory Mx149.
- PE2 (PE10) VIM Mx149 (109):** Processing Element 2 (PE10) Vector Instruction Memory Mx149.
- PE3 (PE11) VIM Mx149 (110):** Processing Element 3 (PE11) Vector Instruction Memory Mx149.

Connections:

- The DMA unit (181) is connected to the MCB (191) and the data bus (121).
- The MCB (191) is connected to the data bus (121) and the SP/PE0 (101) block.
- The SP/PE0 (101) block is connected to the data bus (121) and the I-FETCH-Xpand UNIT (103).
- The I-FETCH-Xpand UNIT (103) is connected to the SP B-BIT INSTRUCTION MEMORY (105) and the PE 32b DATA MEMORY (123').
- The PE 32b DATA MEMORY (123') is connected to the PE LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS (157).
- The PE LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS (157) is connected to the PE CONFIG. REGISTER FILE (151) and the STORE, LOAD, ALU, MAU, DSU block.
- The STORE, LOAD, ALU, MAU, DSU block is connected to the INSTR. DECODE & iVLW CONTROL block.
- The INSTR. DECODE & iVLW CONTROL block is connected to the PE1 (PE01) VIM Mx149 (108), PE2 (PE10) VIM Mx149 (109), and PE3 (PE11) VIM Mx149 (110).
- The PE1 (PE01) VIM Mx149 (108), PE2 (PE10) VIM Mx149 (109), and PE3 (PE11) VIM Mx149 (110) are connected to the data bus (126).



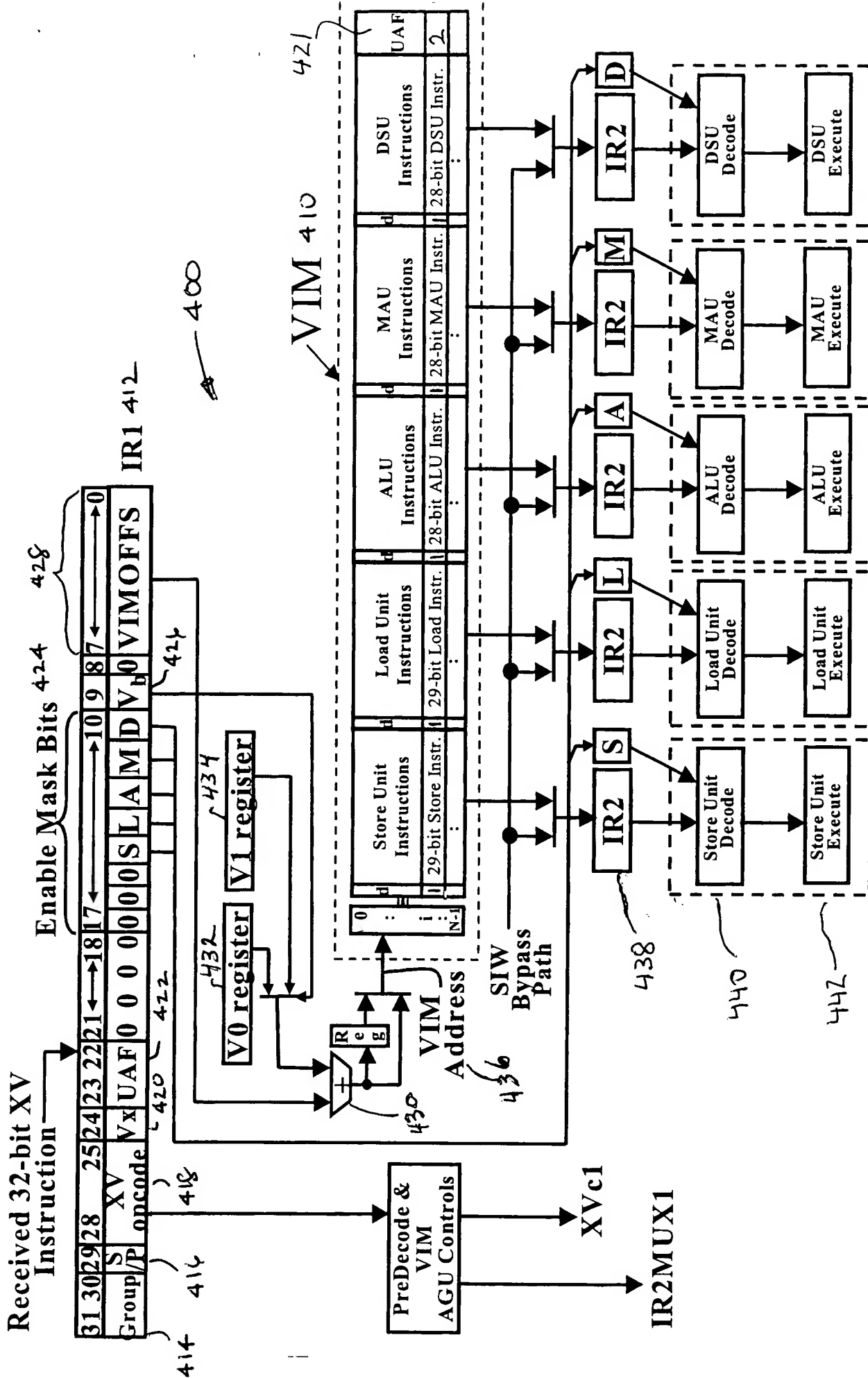


Fig. 4

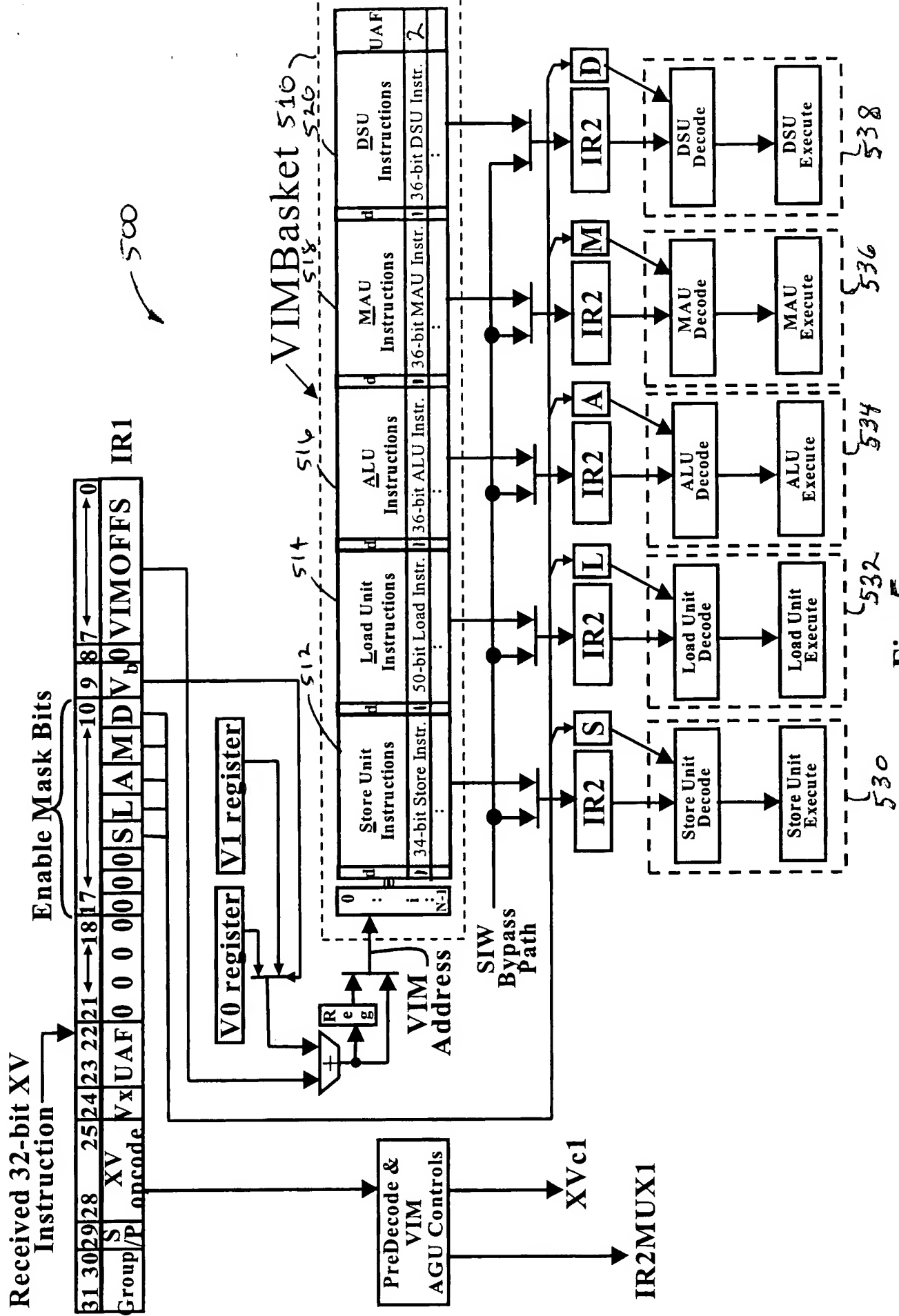


Fig. 5

32-bit Encoding

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group				S/P				Unit				MAUopcode				Rt		Rx				Ry		CE3				SumpExt			
																Rte		0		Rxe		0									

Fig. 6A PRIOR ART

SLAMDunk 40-bit Encoding Example

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group				S/P				Unit				MAUopcode'				Rt'				Rx'				Ry'				CE3				SumpExt'							
																Rte'				0				Rxe'				0				Rye'				0			

Fig. 6B

Fig. 6B

32-bit Mapping to SLAMDunk 40-bit Encoding Example

32-bit Mapping to 32-Bit Link 40-bit Encoding Example																																																			
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0												
Group				S/P				Unit				MAUopcode				0				0				0				0				Rt				Rx				Ry				CE3				SumpExt			
																0				0				0				0				0				0				0				0				0			

Fig. 6C

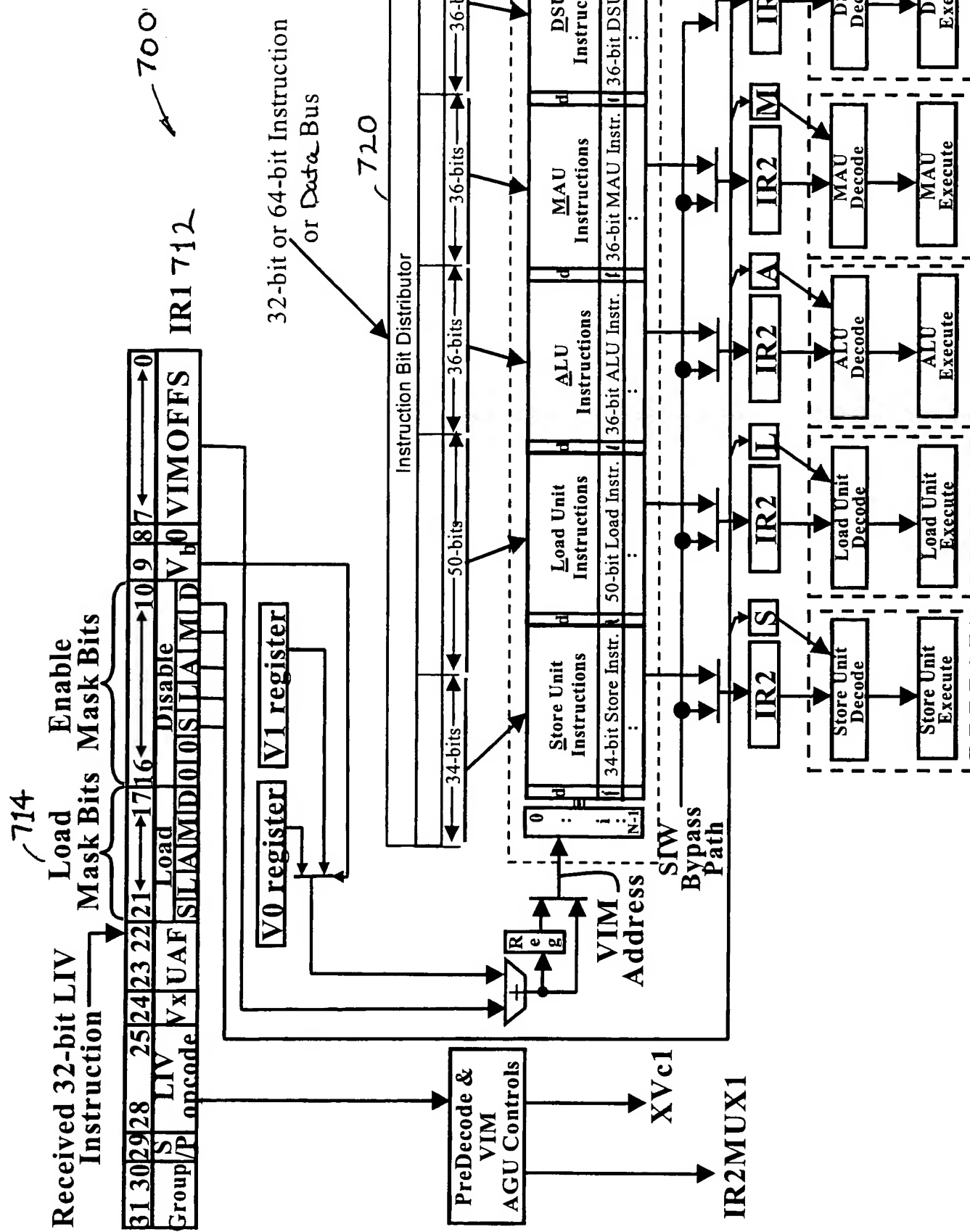
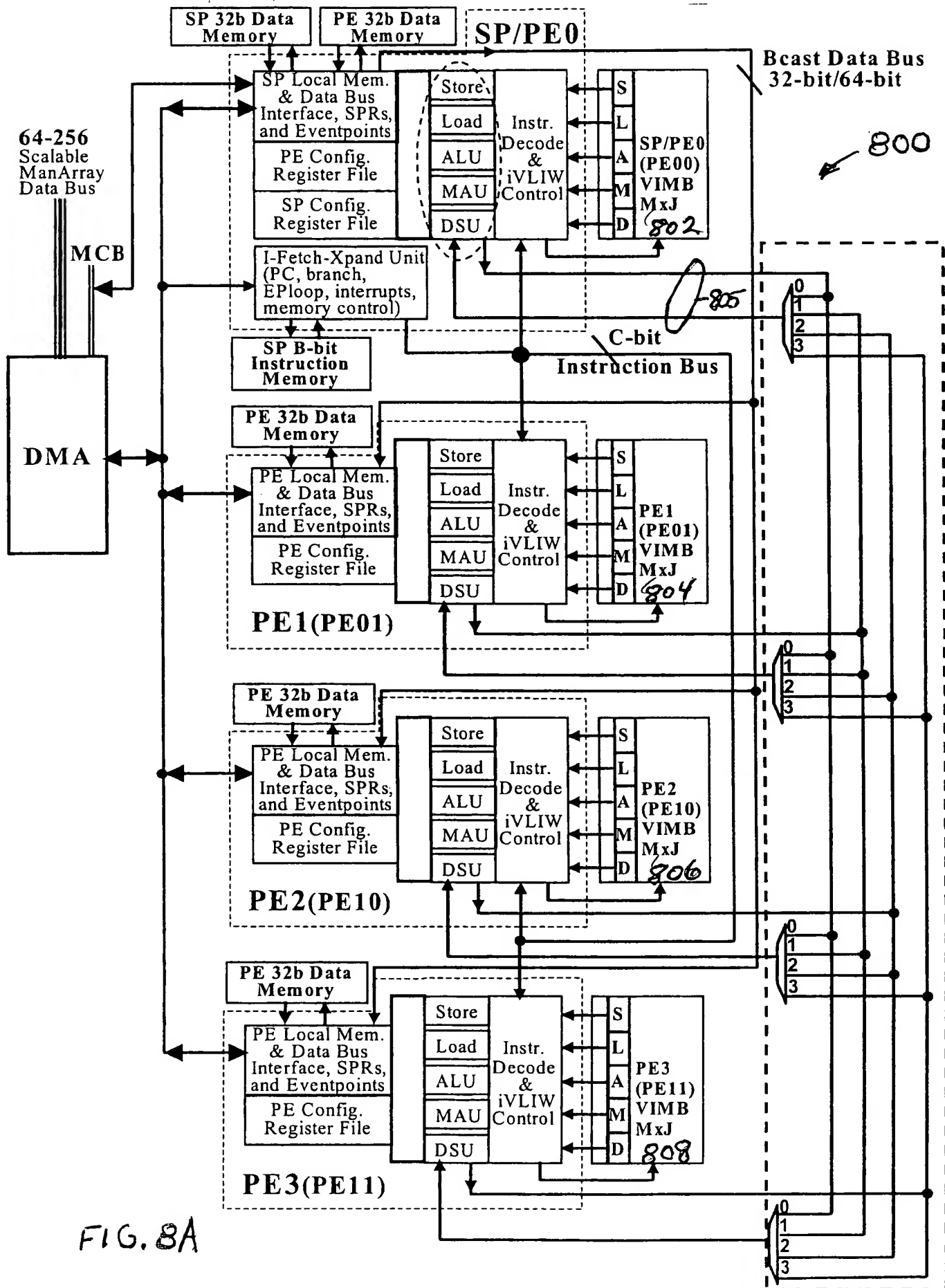
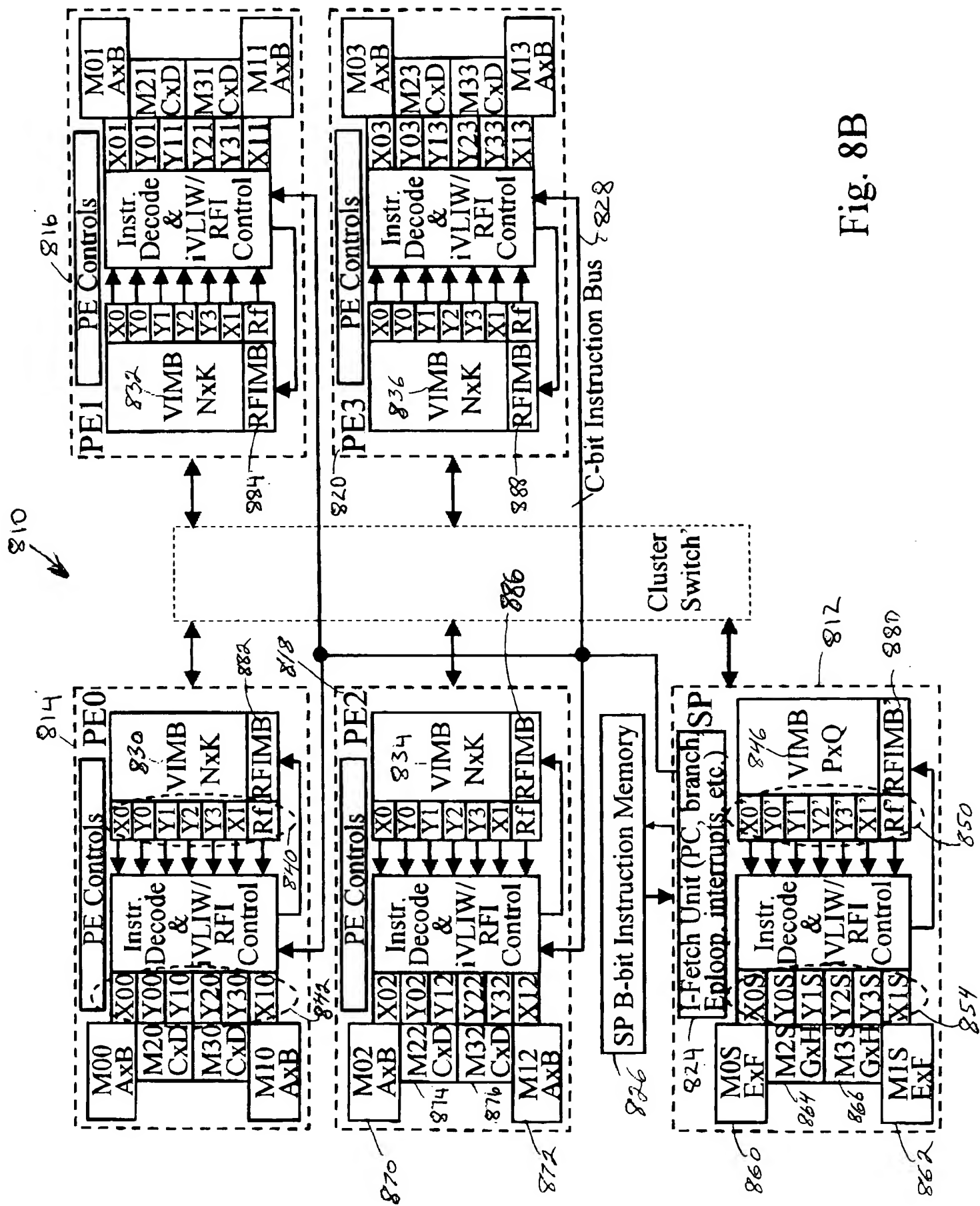


Fig. 7





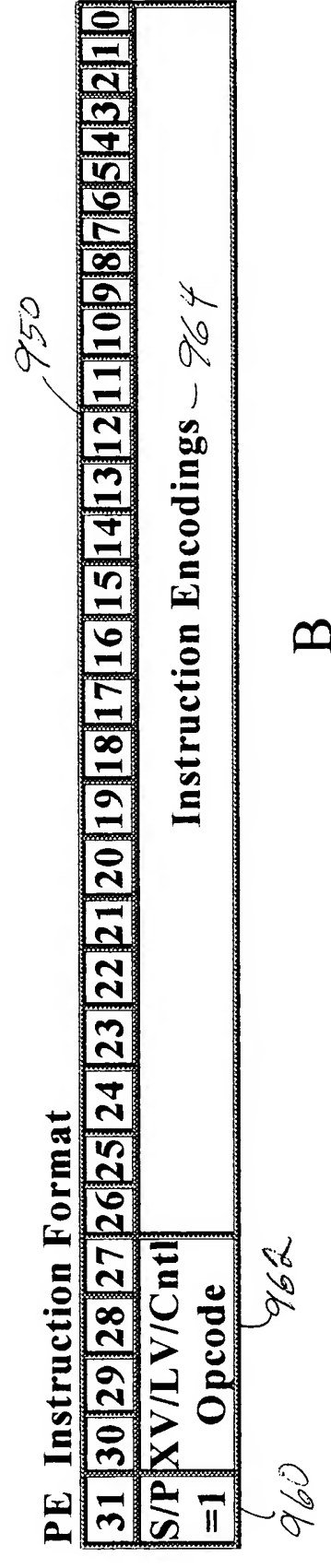
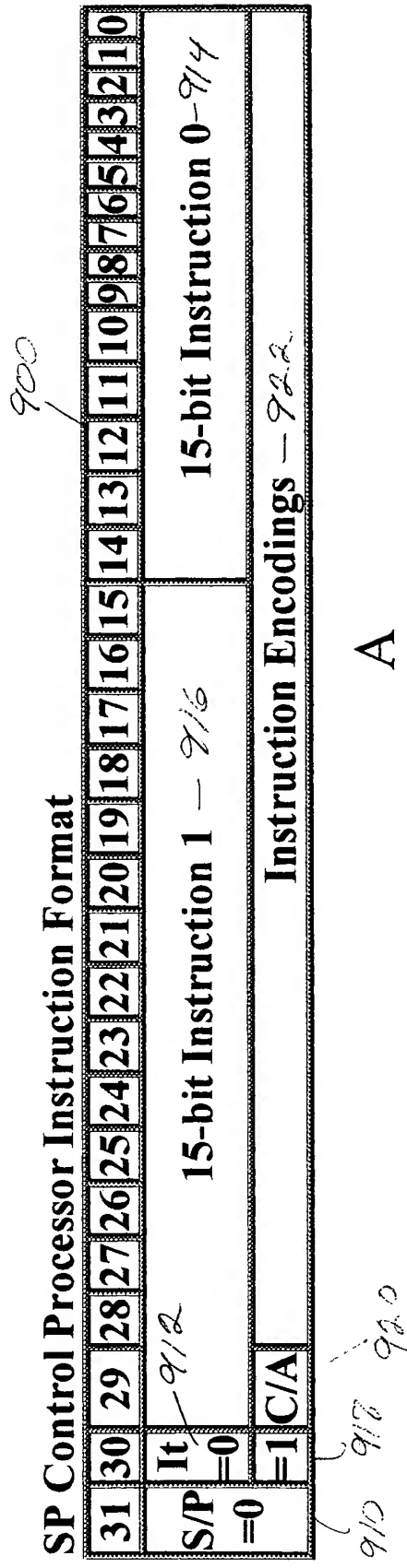
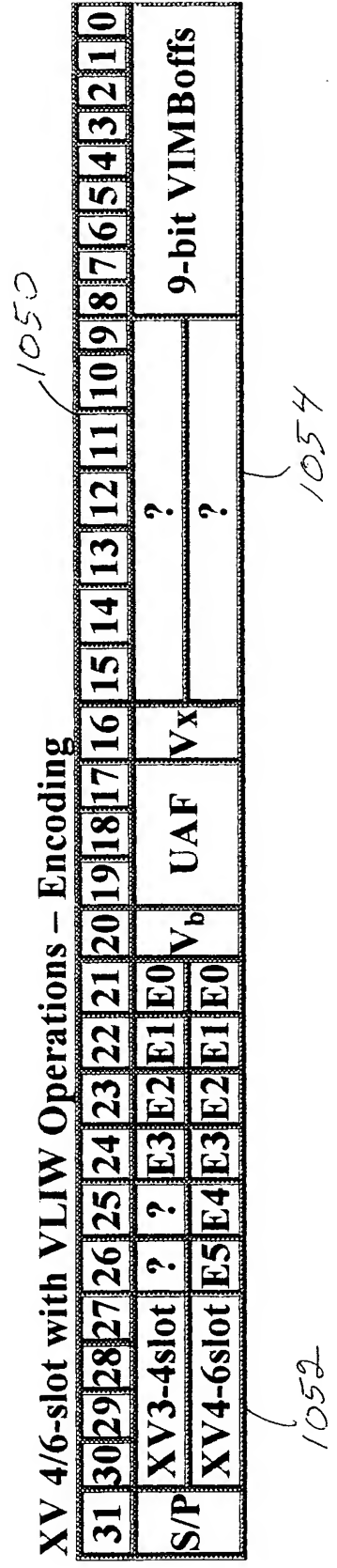
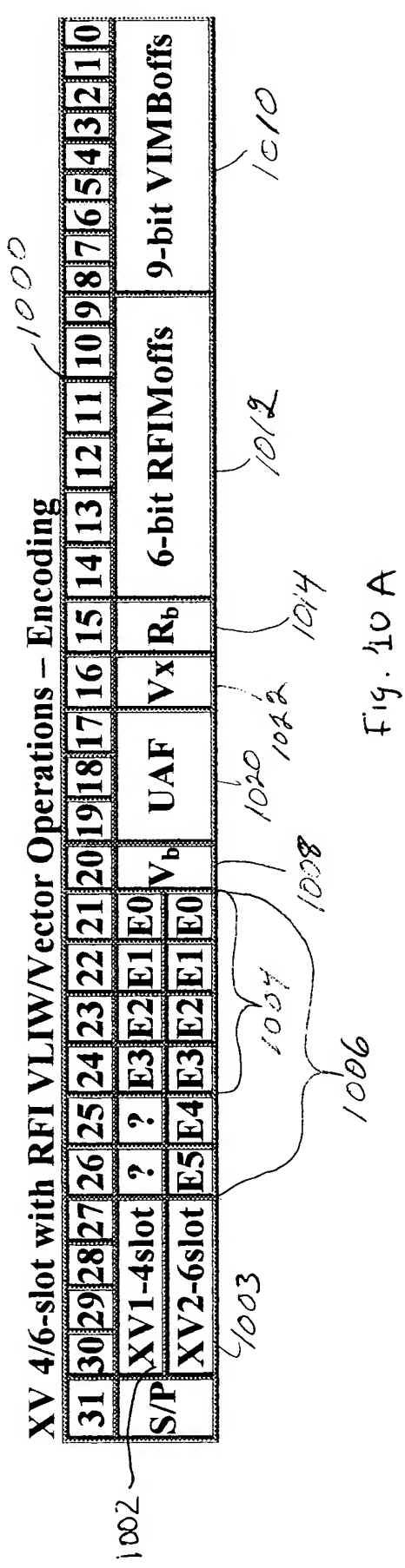
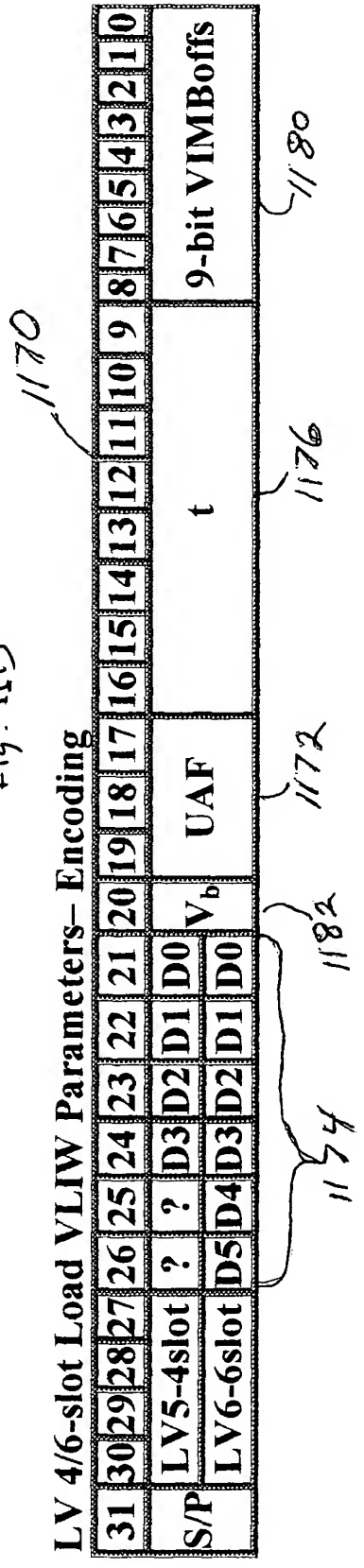
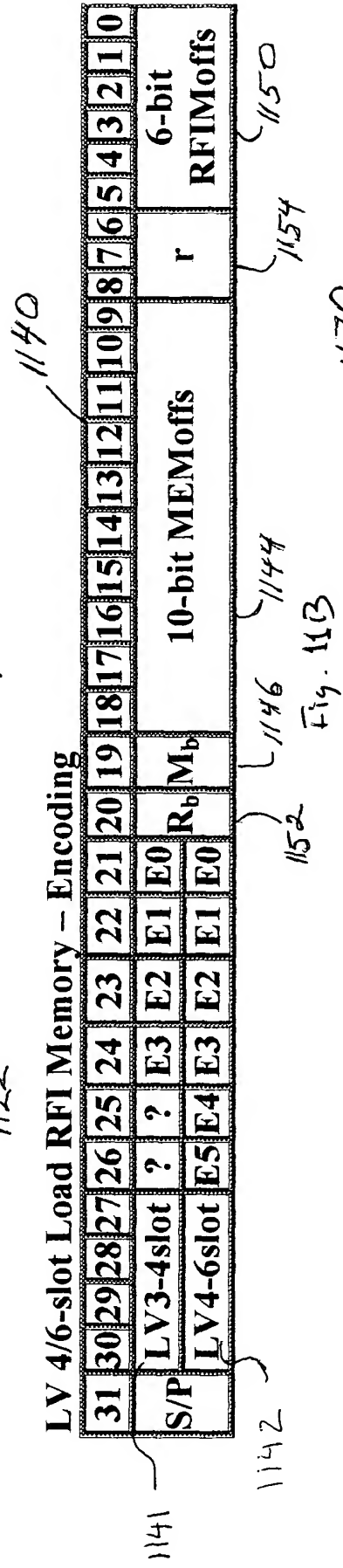
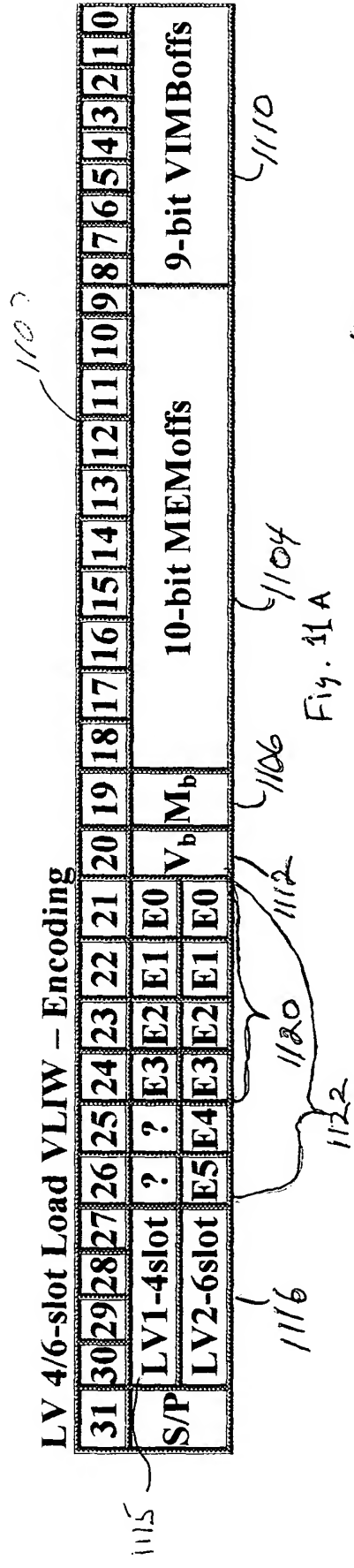
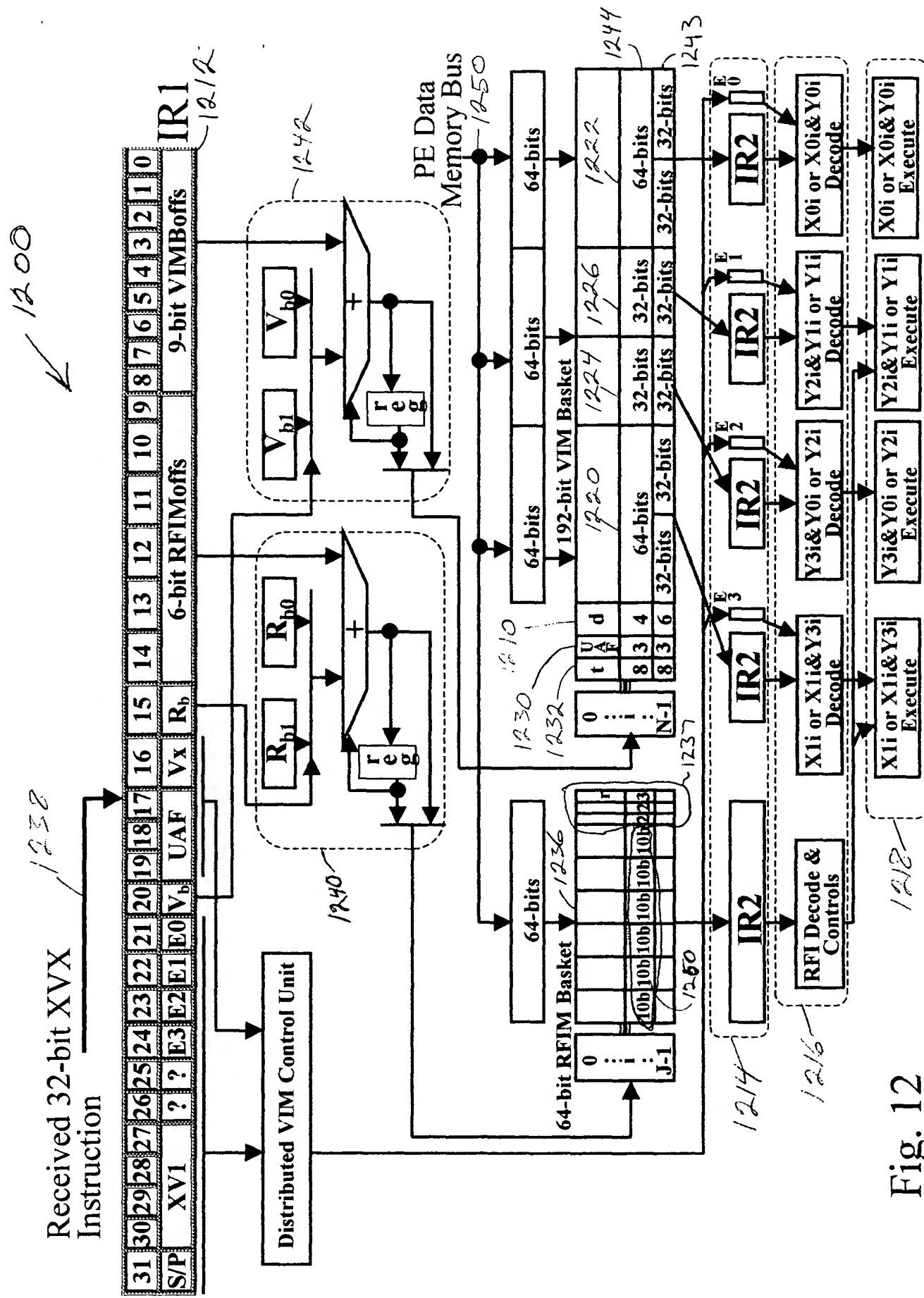


Fig. 9







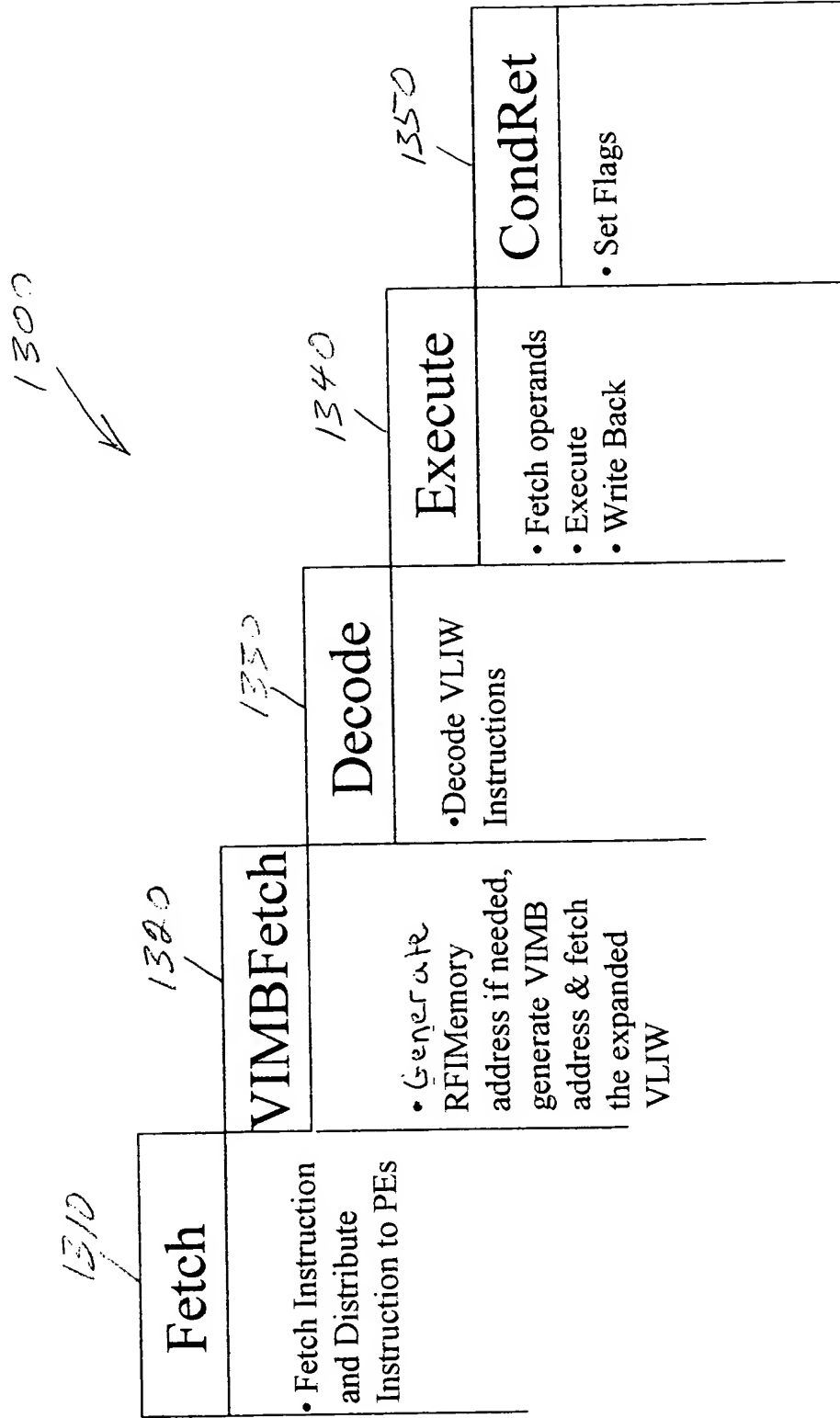


Fig. 13

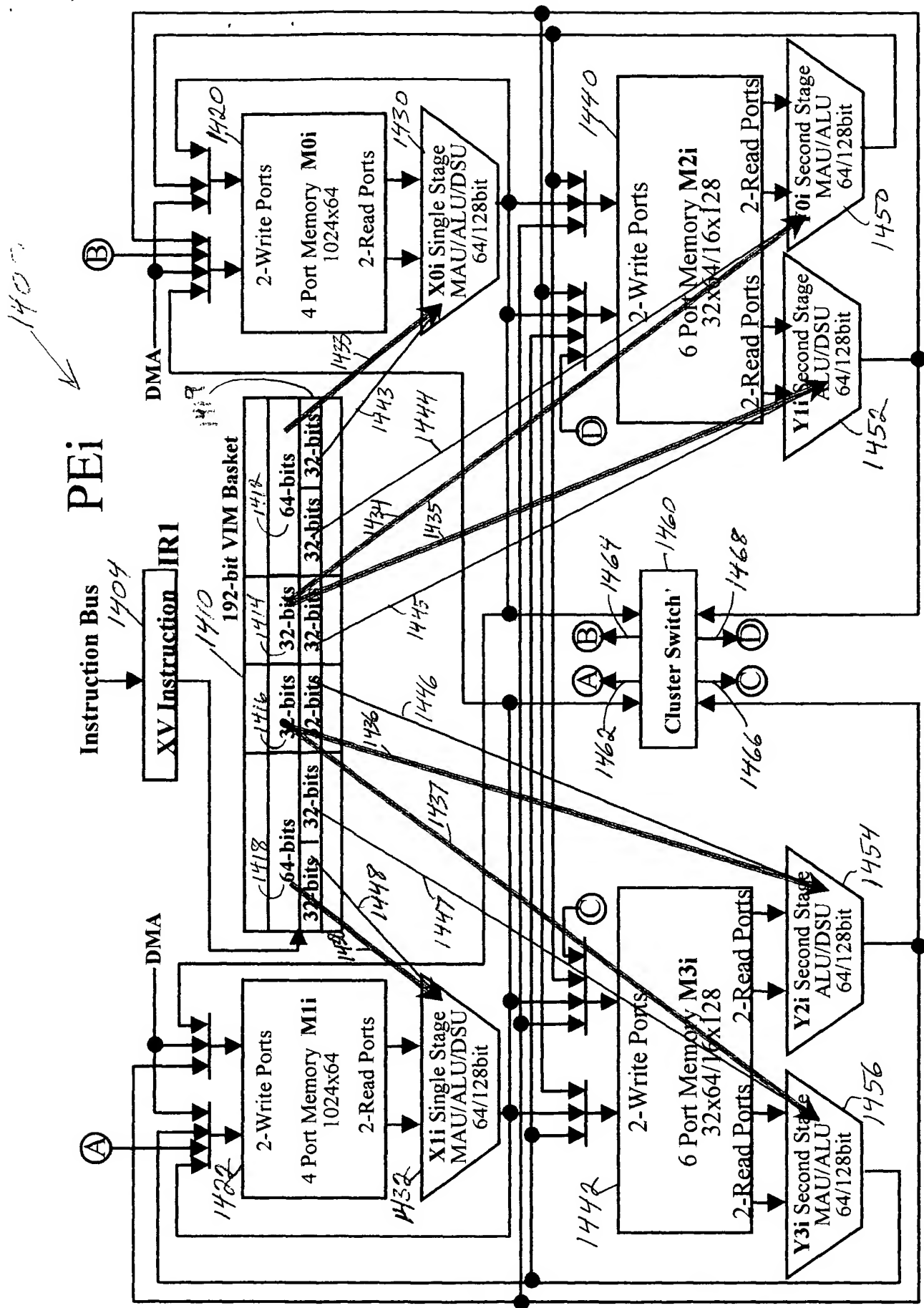


Fig. 14

1500

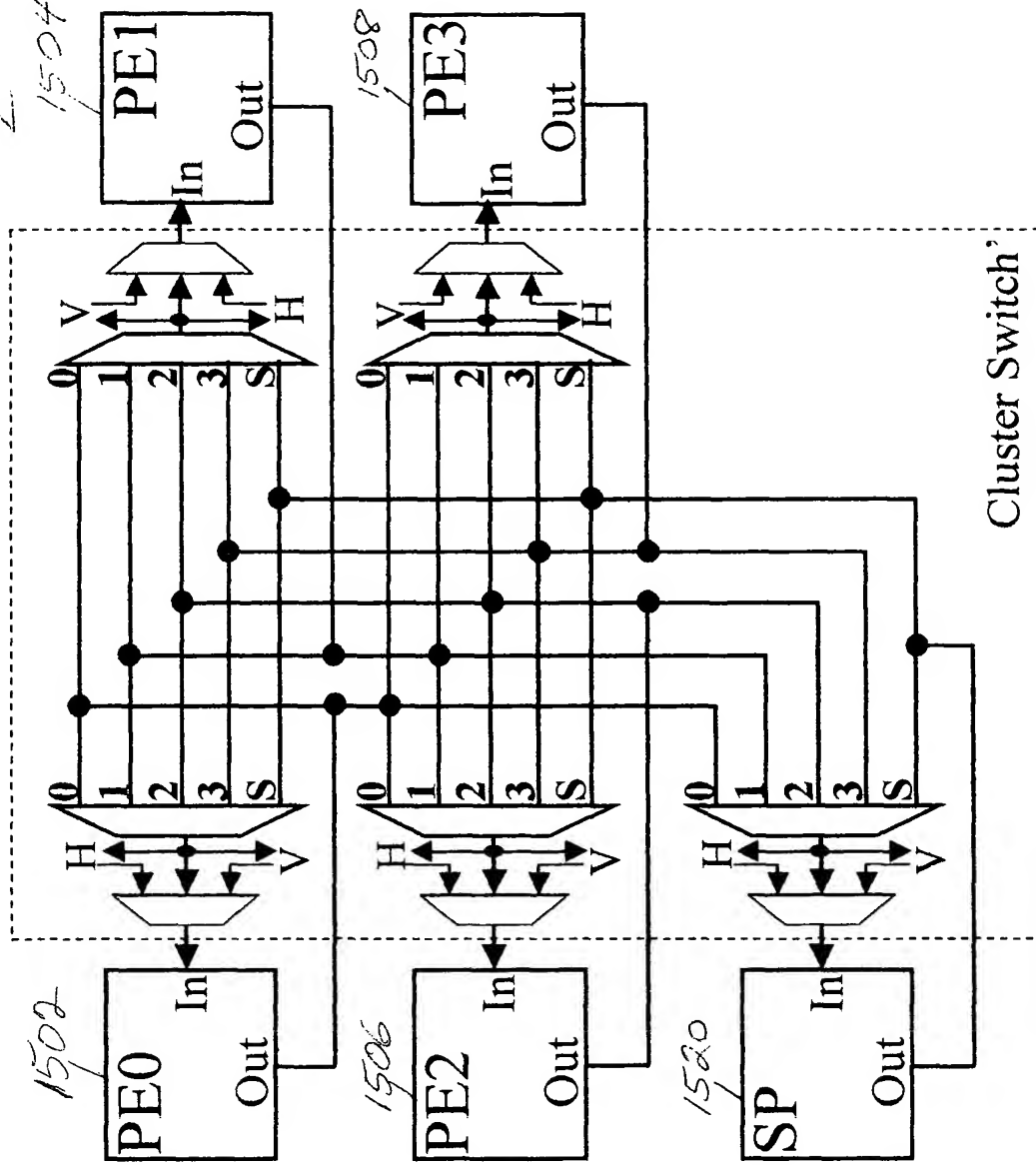


Fig. 15

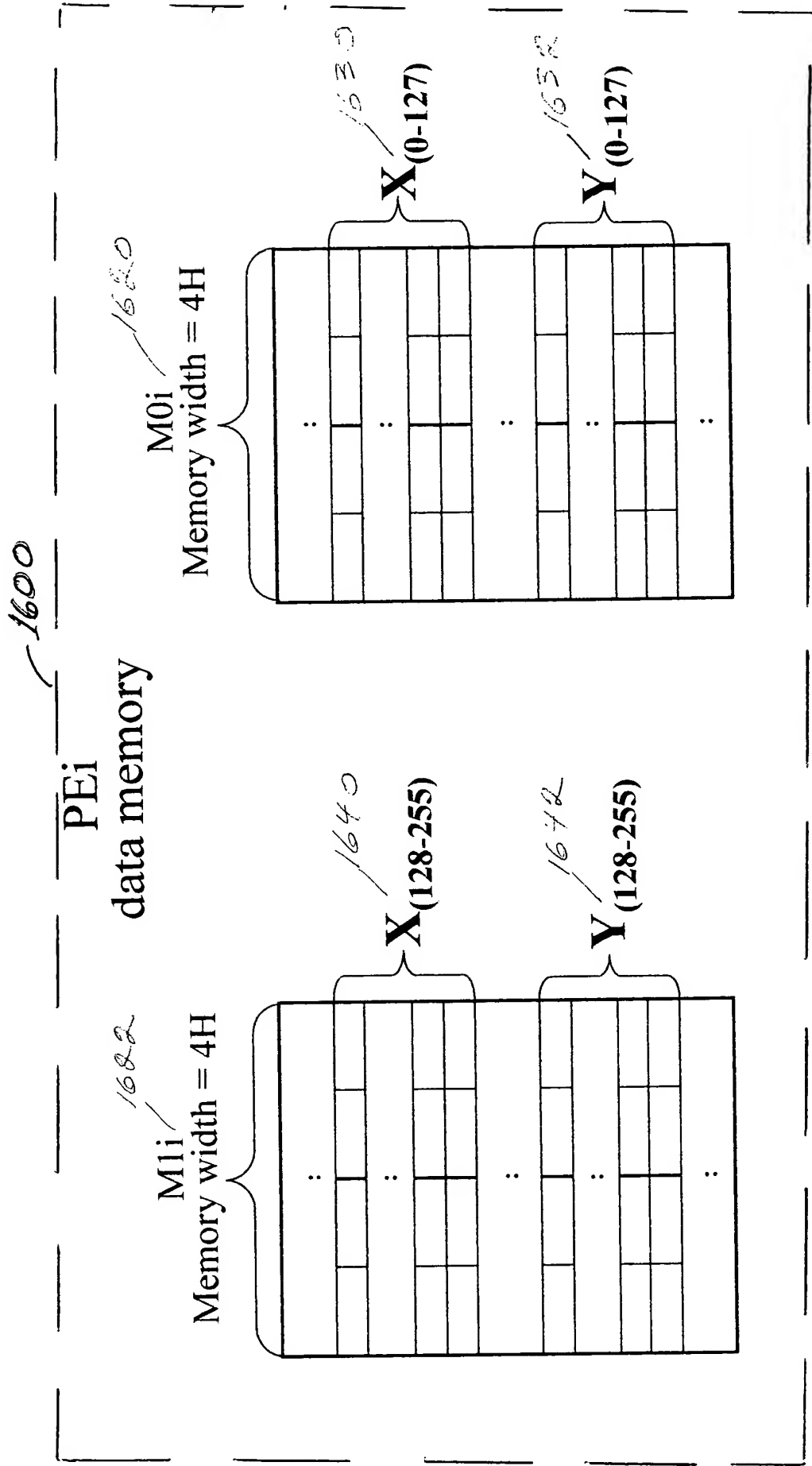


Fig. 16

1700 ✓

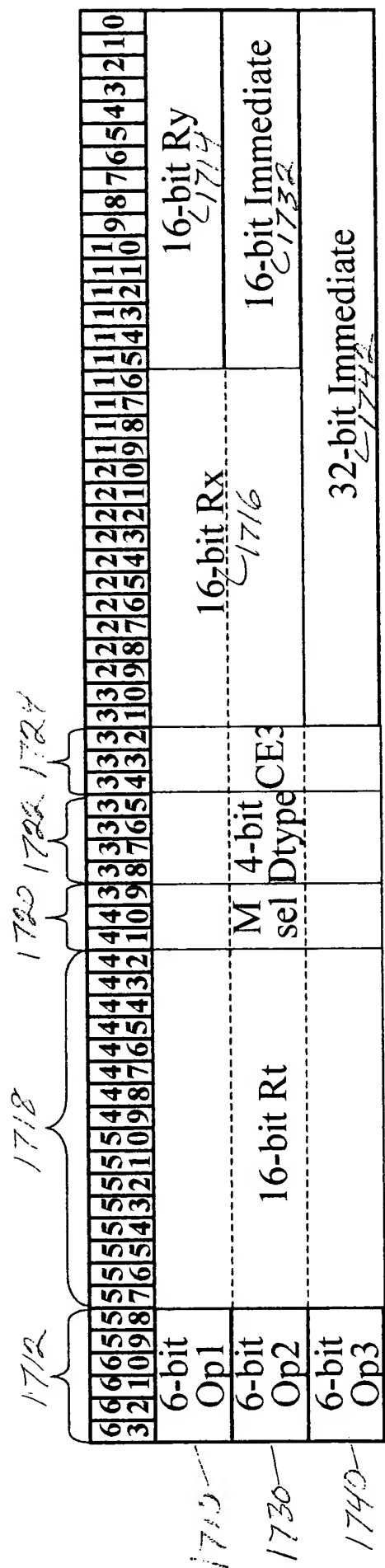


Fig. 17

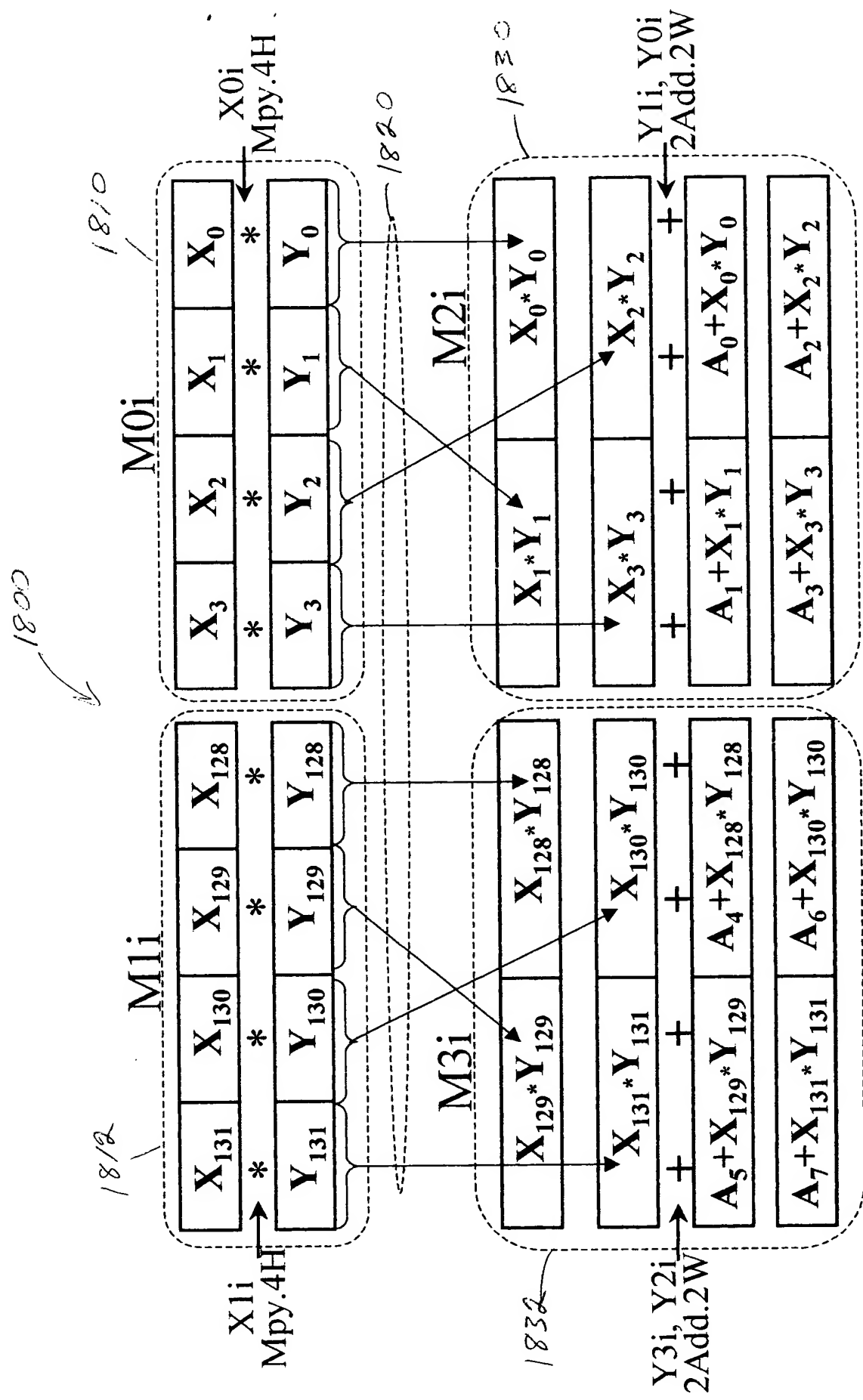


Fig. 18

1900

PE: VIMB VLIW Execution

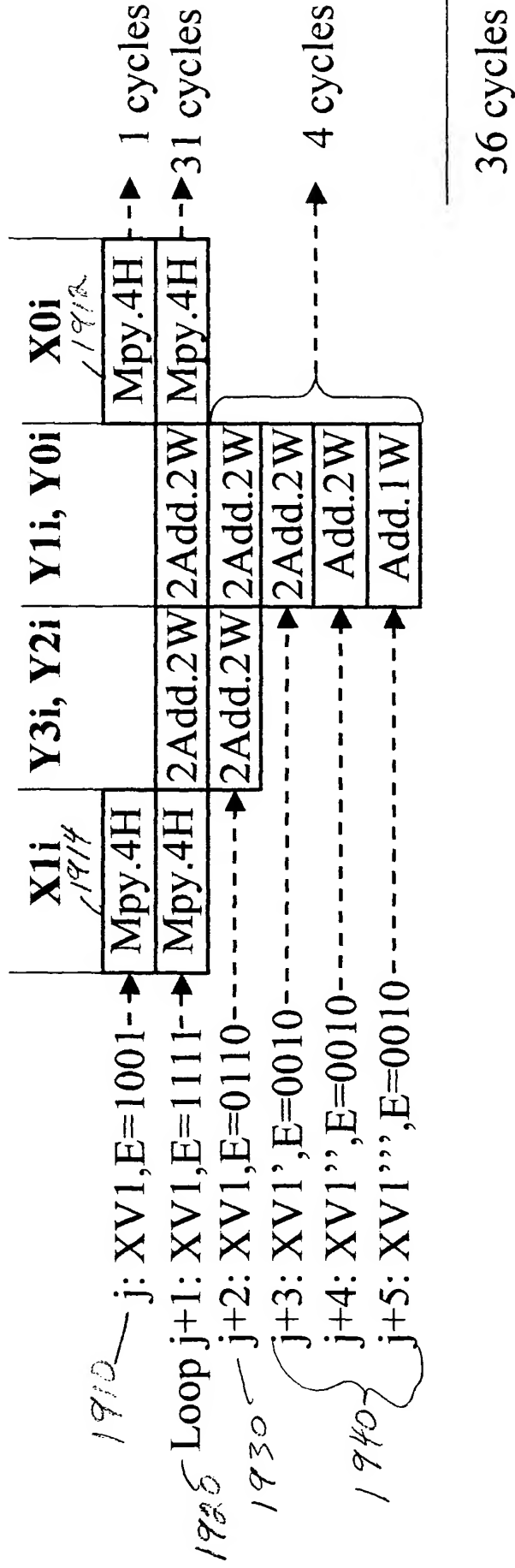


Fig. 19